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UTILITY PATENT APPLICATION FOR:

POWER MANAGEMENT FOR A PIPELINED CIRCUIT

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POWER MANAGEMENT FOR A PIPELINED CIRCUIT

FIELD OF THE INVENTION

The present invention is generally related to power management techniques for computer chips. More particularly, the present invention is generally related to reducing power

5 consumption of a pipelined circuit in a computer chip.

BACKGROUND OF THE INVENTION

In a typical microprocessor chip, designers often use a pipelined circuit to perform certain operations, such as floating point computations, for increasing the chip's frequency. A pipelined circuit conventionally includes multiple pipeline stage circuits for performing the computations. Conventional pipeline stage circuits are often modified to increase the performance of the chip. However, high-performance pipeline stage circuits often substantially dissipate power when performing calculations. Even when functioning in an idle or sleep mode, conventional pipeline stage circuits dissipate a significant amount of power through leakage paths.

With the ever increasing demand for power in microprocessor chips, it is imperative that the power efficiency of every circuit in a microprocessor chip. Accordingly, techniques have been developed for reducing power consumption in microprocessor chips, such as placing pipeline stage circuits in a sleep mode. Techniques utilizing a sleep mode, however, tend to suffer from step-load problems. These problems result from an inductive effect in a power delivery line for the pipeline stage circuits. When pipeline stage circuits are waking up after

20 being in a sleep mode, the circuits usually draw a large amount of current in a short period of time to sustain high-speed operation. This results in a step-load effect.

In order to overcome the step-load effect, an on-chip decoupling capacitance is enlarged or a dummy cycle is introduced in the pipeline stage circuits to prevent an inductive spike. Enlarging the on-chip decoupling capacitance, however, has not proved feasible for a variant

25 demand for power during chip operation. Also, executing a dummy cycle tends to waste a considerable amount of power.

SUMMARY OF THE INVENTION

In one respect, the present invention includes a method for minimizing power consumption by a circuit, such as a pipelined circuit. The method includes steps of determining whether a predetermined period of time has expired, and performing a shut-down procedure on

5   the pipelined circuit in response to the predetermined period of time having expired or elapsed. The predetermined period of time is associated with a predetermined period of time to detect a transition of a signal output by the pipelined circuit.

In another respect, the present invention includes a circuit operable to minimize power consumption by a pipelined circuit. The circuit includes a first transition detection circuit connected to a first bus and detecting transition of a signal on the first bus. The first bus is operable to carry a signal output by the pipelined circuit. A second transition detection circuit is connected to a second bus and detects transition of a signal on the second bus. The second bus being operable to transmit a signal to the pipelined circuit. A stage control circuit is connected to the first and second transition detection circuits, and the stage control circuit controls the power consumption of the pipelined circuit based on a signal received from either the first transition detection circuit or the second transition detection circuit.

In another respect, the present invention includes a circuit connected to a pipelined circuit. The circuit is operable to control power provided to the pipelined circuit, and the circuit includes a timer, a first sequencer, a second sequencer and an arbitration circuit connected to the

20   first and second sequencers. The arbitration circuit is operable to generate signals for controlling power provided to the pipelined circuit.

In comparison to known prior art, certain embodiments of the invention are capable of achieving certain advantages, such as reducing power consumption and minimizing a step-load effect caused by an instant shut-down or power-up of an entire pipelined circuit. Those skilled in

25   the art will appreciate these and other advantages and benefits of various embodiments of the invention upon reading the following detailed description of a preferred embodiment with reference to the below-listed drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures in which like numeral references refer to like elements, and wherein:

Fig. 1 illustrates an exemplary schematic block diagram of a power control circuit according to an embodiment of the present invention;

Fig. 2 illustrates a timing diagram for a power shut-down procedure utilizing the power control circuit shown in Fig. 1;

Fig. 3 illustrates a timing diagram for a power turn-on procedure utilizing the power control circuit shown in Fig. 1;

Fig. 4 illustrates an exemplary schematic block diagram of an embodiment of the stage power control circuit shown in Fig. 1;

Figs. 5(a)-(c) illustrate detailed schematic block diagrams of the stage power control circuit shown in Fig. 1; and

Fig. 6 illustrates a flow chart of an exemplary method employing the principles of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one of ordinary skill in the art that these specific details need not be used to practice the present invention. In other instances, well known structures, interfaces, and processes have not been shown in detail in order not to unnecessarily obscure the present invention.

Fig. 1 illustrates a power control circuit 100 managing power consumption and power delivery to a pipelined circuit 110. The pipelined circuit 110 includes multiple stage circuits 112, each of which includes a power switch P_N, conventional combinational logic circuitry 116 and a flip-flop 118. The flip-flop 118 may be a conventional flip-flop or a power saving flip-flop

described in co-pending U.S. Patent Application No. TBD (Attorney Docket No. 10015036), herein incorporated by reference.

The power control circuit 100 includes a back-end transition detection circuit 125, a stage power control circuit 130, a front-end transition detection circuit 135 and an optional inserted

5   buffer circuit 140. The front-end transition detection circuit 135 and the back-end transition detection circuit 125 may include conventional circuits for detecting signal transitions on a bus, such as a transition from a high to a low or vice versa. The pipelined circuit 110 may perform data processing, including high-speed computations. The back-end transition detection circuit 125 detects a transition of a signal output by the pipelined circuit 110, such as detecting activity

10   on a bus 150 at the output of the pipelined circuit 110. The activity may include an output of a data computation on the bus 150 from the pipelined circuit 110. The bus 150 may also connect each stage circuit 112 and may carry signals input to the pipelined circuit 110. Alternatively, multiple busses may be used to carry data to/from the pipelined circuit 110 and to interconnect the stage circuits 112. When a transition is not detected by the front-end transition detection

15   circuit 135 or the back-end transition detection circuit 125 for a predetermined period of time, the stage power control circuit 130 sequentially controls power switches P_1-P_N to suppress power supplied to the stage circuits 112. For example, stage power control circuit 130 sequentially opens switches P_1-P_N, starting from the front-end of the pipelined circuit 110 (i.e., at the stage circuit 112 where the data is first input to the pipelined circuit 110). Each power switch P_N may

20   be opened at predetermined intervals to reduce the risk of causing an inductive spike that may result in the step-load effect.

Fig. 2 illustrates a timing diagram for a power shut-down procedure performed by the stage power control circuit 130. For each clock cycle, the stage power control circuit 130 suppresses power, for example, by opening a power switch P_N connected to a stage circuit 112,

25   starting from the front-end of the pipelined circuit 110. For example, upon the detection of a shut-down command (e.g., a signal indicating that the predetermined period of time for transition detection circuits 125 and 135 to detect a transition has expired) in the first cycle T_0, the stage power control circuit 130 generates a signal to open switch P_1 at the time T_1. Then, at the end of a second clock cycle T_2 and a third clock cycle T_3, the stage power control circuit generates

30   signals to open switches P_2 and P_3 respectively. The switches P_1-P_N may sequentially be opened

until the last switch P_N is opened at T_N. Then, the pipelined circuit 110 is in a sleep mode and consumes minimal power.

When the front-end transition detection circuit 135 detects bus activity on the bus 150, such as when new data is received by the pipelined circuit 110 on the bus 150, the front-end transition detection circuit 135 transmits a wake-up signal to the stage power control circuit 130. Then, the stage power control circuit 110 sequentially controls power switches P_1-P_N to supply power to the stage circuits 112. For example, stage power control circuit 130 sequentially closes switches P_1-P_N, starting from the front-end of the pipelined circuit 110 (i.e., at the stage circuit 112 where the data is first input to the pipelined circuit 110). Each power switch P_N may be closed at predetermined intervals.

Fig. 3 illustrates a timing diagram for a power turn-on procedure performed by the stage power control circuit 130. For each clock cycle, the power control stage circuit 130 controls a power switch P_N, such that power is supplied to each stage circuit 112 starting from the front-end of the pipelined circuit 110. For example, upon the detection of the front end bus transition in the first cycle C_0, the stage power control circuit 130 generates a signal to close switch P_1 at the time C_1. Then, at the end of a second clock cycle C_2 and a third clock cycle C_3, the stage power control circuit 130 generates signals to close switches P_2 and P_3 respectively. The switches P_1-P_N may sequentially be closed until the last switch P_N is closed at C_N. Then, the pipelined circuit 110 is operable to perform data computations at each stage circuit 112.

In one embodiment, the circuit 100 may optionally include a buffer circuit 140. Because the transition detection circuits 125 and 135 and the stage control circuit 130 take time to respond to detected transitions, it may be necessary to insert the buffer circuit 140 in the front end of the pipelined circuit 110 to buffer the incoming data. In another embodiment, the buffer circuit 140 is not used in the circuit 100 when the latency of data moving through the pipeline circuit 110 becomes critical. In this case, the first stage circuit (i.e., the stage circuit 112 at the front-end of the pipelined circuit 110) may continually receive power and not include a power switch P_1, and the front-end transition detection circuit 135 may receive a signal input to the first stage circuit. Then, the first stage circuit serves as a buffer for the pipelined circuit 110. This trade-off between power consumption and speed may be determined by the system requirements.

Fig. 4 illustrates an exemplary embodiment of the stage power control circuit 130, shown in Fig. 1. The stage power control circuit 130 includes a wake-up/shut-down arbitration circuit 410, a wake-up step sequencer 420, a shut-down step sequencer 430 and a programmable timing interval counter 440. The programmable timing interval counter 440 includes a timer for

5 measuring a predetermined period of time before the pipelined circuit 110 may be placed in sleep mode. The back-end transition detection circuit 125, shown in Fig. 1, transmits a signal to the reset input of the programmable timing interval counter 440 when a transition is detected. This causes the programmable timing interval counter 440 to restart the timer. If the programmable timing interval counter 440 is not reset by the back-end transition detection circuit 125 prior to

10 expiration of the timer (i.e., the back-end transition detection circuit 125 does not detect a transition within the predetermined period of time), the programmable timing interval counter 440 transmits a shut-down signal to the shut-down step sequencer 430. Then, the shut-down step sequencer 430 transmits a signal to the wake-up/shut-down arbitration circuit 410, and the wake-up/shut-down arbitration circuit 410 sequentially generates signals for opening switches P_1-P_N.

15 The front-end transition detection circuit 135 may output a signal to the reset input of the programmable timing interval counter 440, similarly to the transmission signal of the back-end transition detection circuit 125, when a transition is detected to reset the counter.

The wake-up step sequencer 420 receives a signal from the front-end detection circuit 135 when the front-end detection circuit 135 detects a transition. Then, the wake-up step

20 sequencer transmits a signal to the wake-up/shut-down arbitration circuit 410, causing the wake-up/shut-down arbitration circuit 410 to sequentially generate signals for closing switches P_1-P_N.

The wake-up/shut-down arbitration circuit 410 may include a multiplexer (not shown) for selecting wake-up/shut-down sequential signals to control each of switches P_1-P_N and an arbitrator (not shown) for determining which sequence(wake up or shut down) should take

25 precedence in case of conflict. For example, a wake-up procedure typically takes precedence over a shut-down procedure. However, in order not to aggravate the step load effect, the stage power control circuit 130 may allow the shut-down procedure to temporarily progress while the wake-up procedure is gradually implemented. Also, the programming timing interval counter 440 may include a conventional timer, and the length of the predetermined period of time may be

30 readily determined by one of ordinary skill in the art according to the configuration of the circuit

100 and other known factors. The length of the predetermined period of time may also be dictated by system requirements. The step sequencer circuits 420 and 430 are conventional circuits that may include shift registers and buffers. It will be apparent to one of ordinary skill in the art that the circuits 410-440 may be constructed from known circuits.

5   Figure 5(a) illustrates an exemplary embodiment of the stage power control circuit 130 shown in Fig. 4. The wake-up/shut-down arbitration circuit 410, the wake-up step sequencer 420, and the shut-down step sequencer 430 may be implemented by an up/down sequencer 510, gates 520 for driving power switches P_1-P_N, a multiplexer 530 and a shift enable gate 540. The up/down sequencer 510 may include an N-bit shift register. The up/down sequencer 510 is

10   connected to the multiplexer 530 and the gate 540 for controlling shifting in the up/down sequencer 510. The gate 540 may output a shift enable signal to facilitate shifting the contents of the registers in the up/down sequencer 510. A gate 550 is connected to the programmable timing interval counter 440 for controlling the reset input for the counter 440, and a latch 560 converts a transition detection pulse to a step signal transmitted to the gate 540.

15   The up/down sequencer 510 stores the status of switches P_1-P_N. The multiplexer 530 selects a "1" (up) or a "0" (down) to be shifted into the up/down sequencer 510 based on a signal from the programmable timing interval counter 440.

          As further illustrated in Fig 5(a), when the front-end or back-end transition detection circuits 135 and 125 detect activity (e.g., during an active power mode), "1's" are sequentially

20   shifted into the up/down sequencer 510 to turn on the power switches P_1-P_N. For example, the programmable timing interval counter 440 transmits a wake-up select signal to the multiplexer 530, and the multiplexer selects "1's" for transmission to the up/down sequencer 510.

          As illustrated in Fig. 5(b), "0's" are shifted into the up/down sequencer 510 during a shut-down procedure, such as after a predetermined period of time has expired without a bus

25   transition being detected since the programmable timing interval counter 440 has been reset. For example, the programmable timing interval counter 440 outputs a shut-down select signal to the multiplexer 530, and the multiplexer 530 selects "0's" for transmission to the up/down sequencer 510. When a "0" is shifted into a register in the up/down sequencer 510, a corresponding gate 520 drives the corresponding power switch P_N closed. If the programmable timing interval

counter 440 is not reset, all the power switches P_1-P_N will be sequentially closed. Then, the pipeline circuit 110 is in a power saving mode (i.e., a sleep mode).

If the front-end transition detection circuit 135 then detects activity, the wake-up procedure begins, as illustrated in Fig. 5(c). Then, "1's" are shifted into the up/down sequencer 510, causing the switches P_1-P_N to be sequentially opened. The wake-up procedure may begin prior to all the power switches P_1-P_N being closed.

It will be apparent to one of ordinary skill in the art that the circuit 100 may be configured to conform with certain system specifications in power management, such as the advanced configuration and power interface specification (ACPI). Also, the circuit 100 may be used as a standalone circuit or integrated in another circuit, such as a power management unit of a chip.

Fig. 6 illustrates a method 600 for minimizing power consumption for the pipelined circuit 110. In step 610, the stage power control unit 130 determines whether no transition has been detected by either the front-end or back-end transition detection circuits 135 and 125 has at the input or output of the pipelined circuit 110 prior to the expiration of a predetermined period of time (e.g. 100 clock cycles). It will be apparent to one of ordinary skill in the art that the predetermined period of time may vary according to the configuration of the circuit 100 and other known factors. The length of the predetermined period of time may also be dictated by the system requirements.

In step 615, if no transition was detected prior to the expiration of the predetermined period of time, the stage power control circuit performs a sequential shut-down procedure. This procedure may include sequentially opening switches P_1-P_N, such as opening one switch every clock cycle starting from P_1. Thus, power for each stage circuit 112 is suppressed, and the power consumption is minimized.

If a transition was detected in step 610, prior to the expiration of the predetermined period of time, then the stage power control circuit 130 continues active mode operation until the predetermined period of time has expired.

In step 620, the stage power control circuit 130 determines whether a transition is detected at the input of the pipelined circuit 110 by the front-end transition detection circuit 135. If a transition is detected, the stage power control circuit 130 performs a sequential turn-on procedure (step 625). This procedure may include sequentially closing switches P_1-P_N, such as closing one switch every clock cycle starting at P_1. If all the switches P_1-P_N were not opened prior to the front-end transition detection circuit 135 detecting a transition (e.g., during the sequential shut down procedure performed in the step 615), then the stage power control circuit 130 could close those switches that were opened or wait until all the switches P_1-P_N close and let wake-up signals open switches P_1-P_N gradually.

If a transition is not detected in step 620, the stage power control circuit 130 continues to open the switches P_1-P_N (step 615). For example, one switch may be opened after each clock cycle until all the switches are opened or until the front-end transition detection circuit 135 detects a transition.

The method 600 shown in Fig. 6 and described above may generally be performed by the stage power control circuit 130. The steps in the method 600 can also be performed by a computer program executed by a processor, instead of the stage power control circuit 110. The computer program can exist in a variety of forms both active and inactive. For example, the computer program can exist as software comprised of program instructions or statements in source code, object code, executable code or other formats; firmware program(s); or hardware description language (HDL) files. Any of the above can be embodied on a computer readable medium, which include storage devices and signals, in compressed or uncompressed form. Exemplary computer readable storage devices include conventional computer system RAM (random access memory), ROM (read only memory), EPROM (erasable, programmable ROM), EEPROM (electrically erasable, programmable ROM), and magnetic or optical disks or tapes. Exemplary computer readable signals, whether modulated using a carrier or not, are signals that a computer system hosting or running the computer program can be configured to access, including signals downloaded through the Internet or other networks. Concrete examples of the foregoing include distribution of executable software program(s) of the computer program on a CD ROM or via Internet download. In a sense, the Internet itself, as an abstract entity, is a computer readable medium. The same is true of computer networks in general.

While this invention has been described in conjunction with the specific embodiments thereof, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. There are changes that may be made without departing from the spirit and scope of the invention.